

FIG. 1A

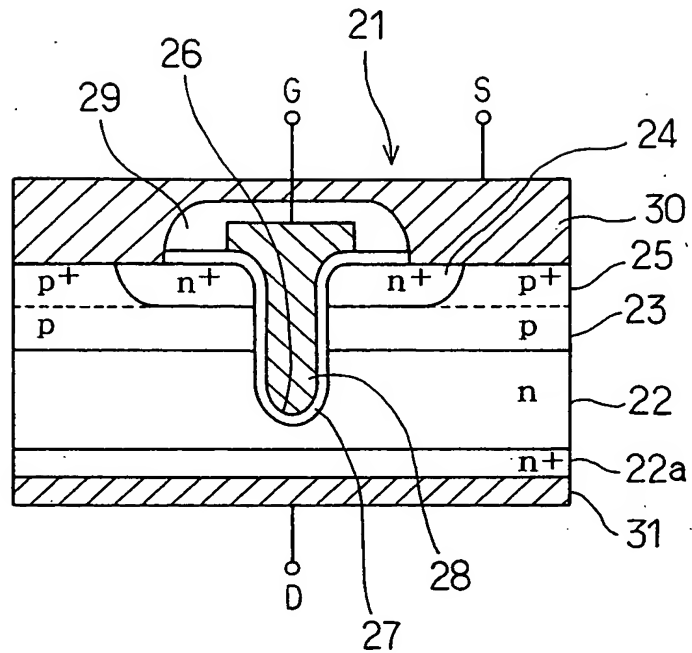


FIG. 1B

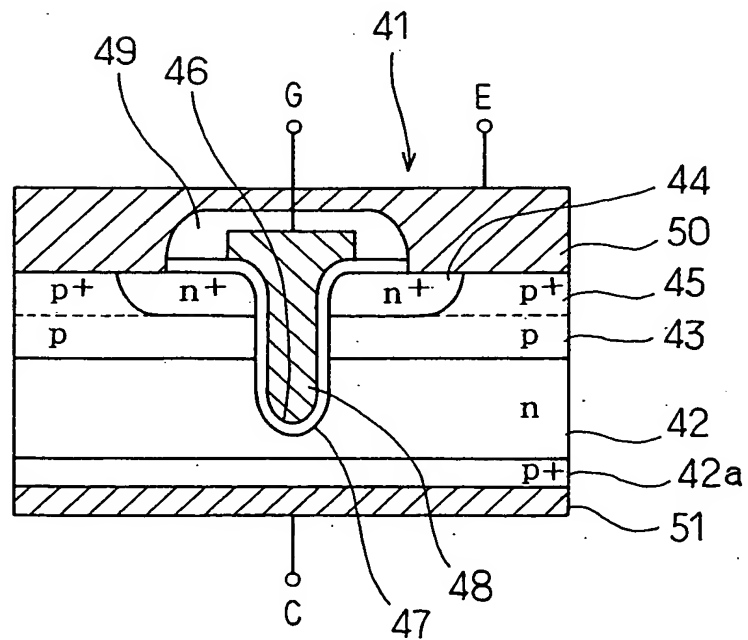


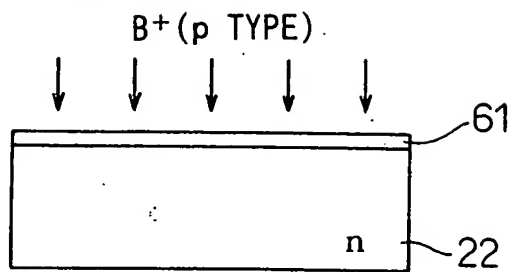
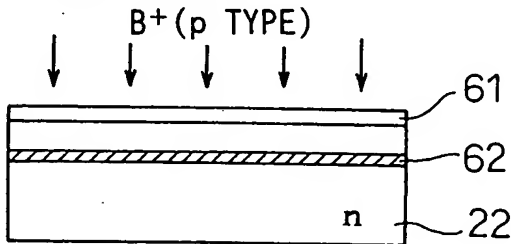
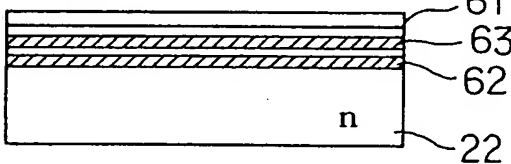
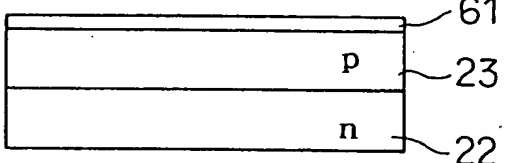
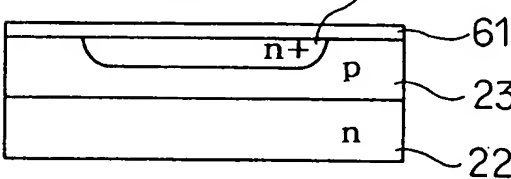
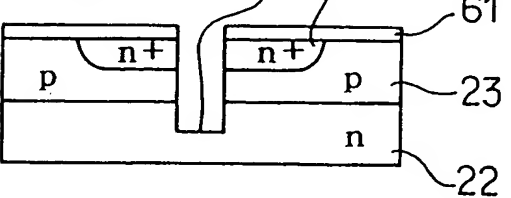
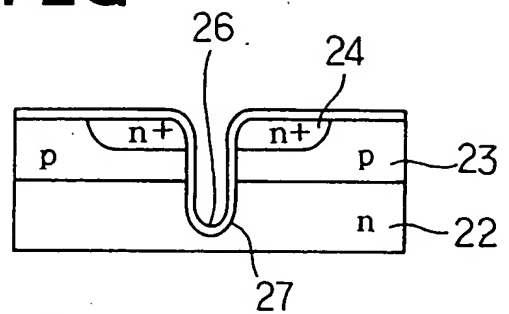
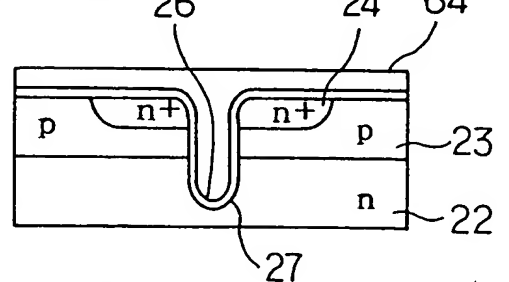
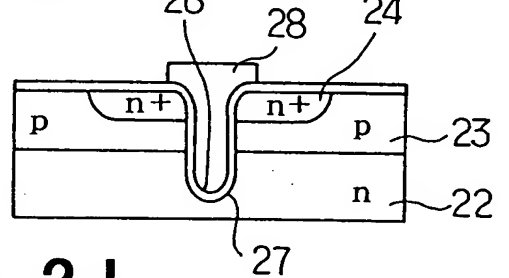
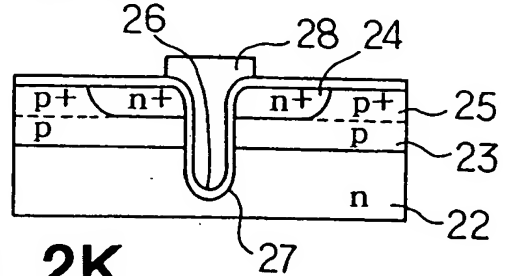
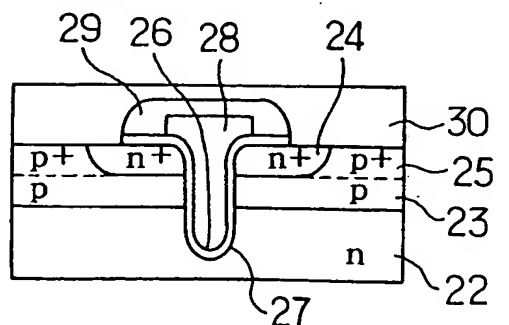
FIG. 2A**FIG. 2B****FIG. 2C****FIG. 2D****FIG. 2E****FIG. 2F****FIG. 2G****FIG. 2H****FIG. 2I****FIG. 2J****FIG. 2K**

FIG. 3A

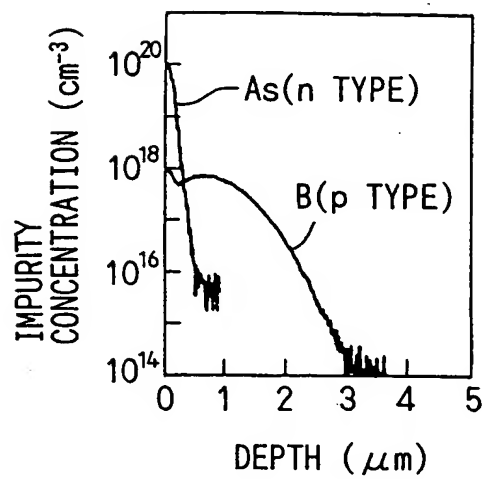


FIG. 3B

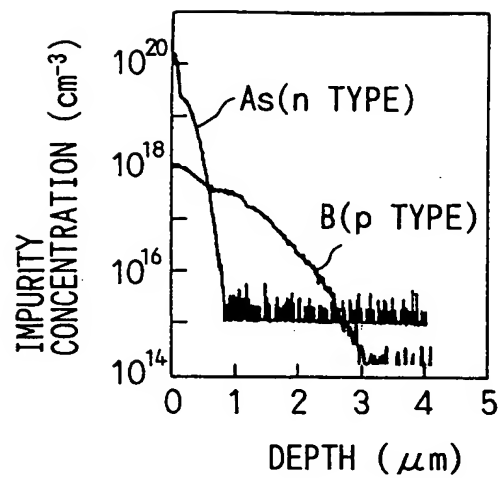


FIG. 4A

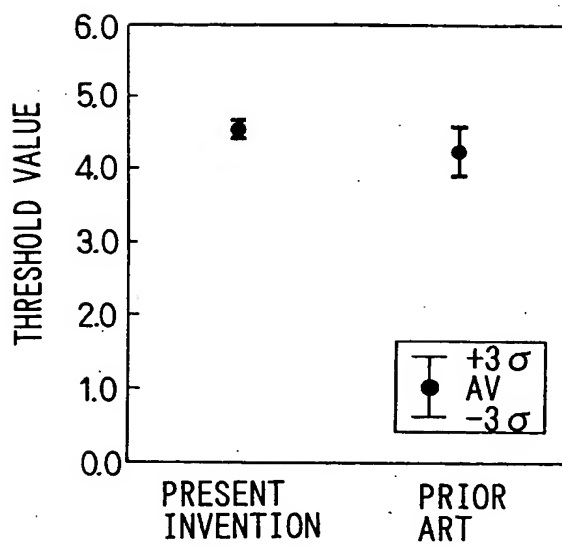


FIG. 4B

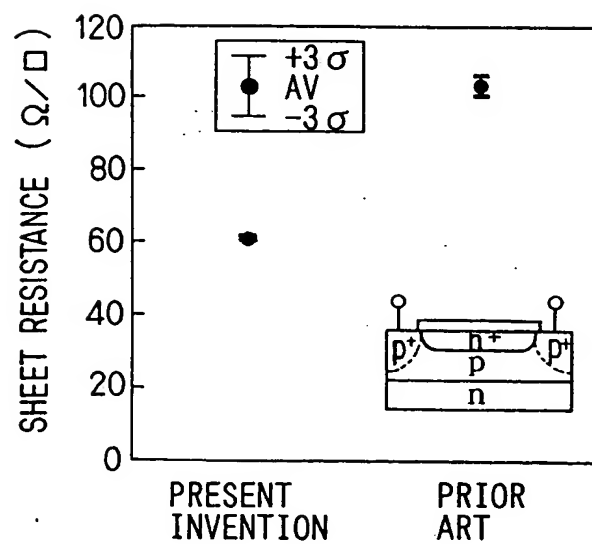


FIG. 5

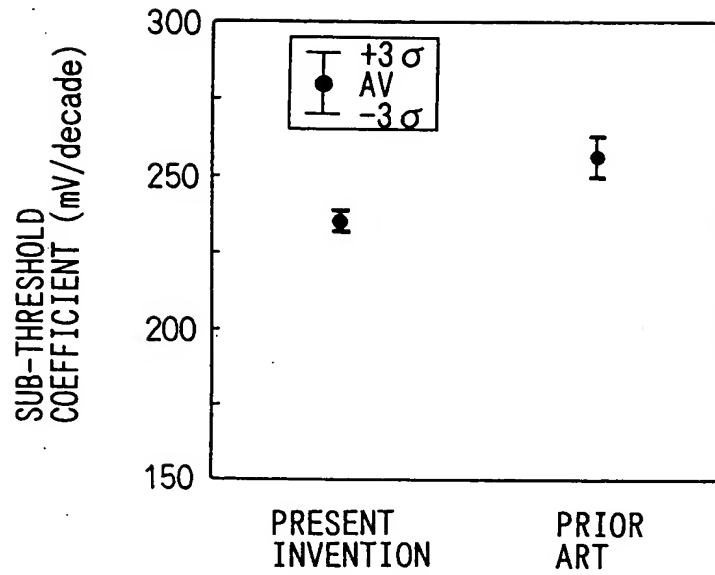


FIG. 6

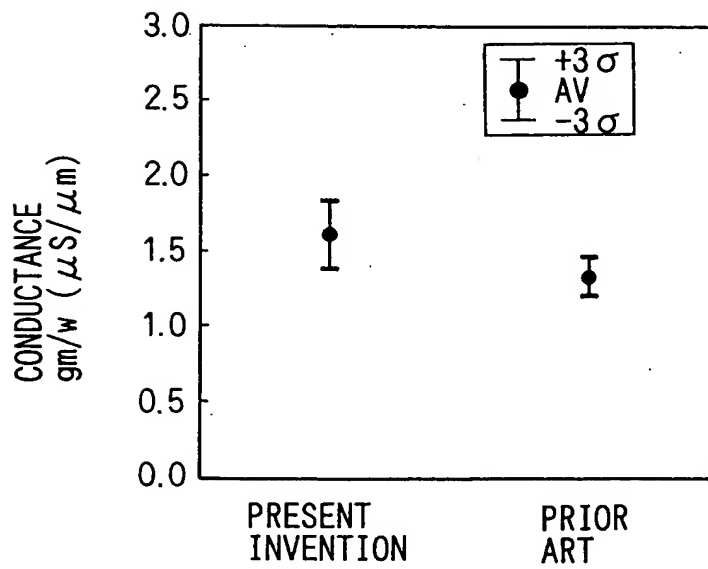


FIG. 7

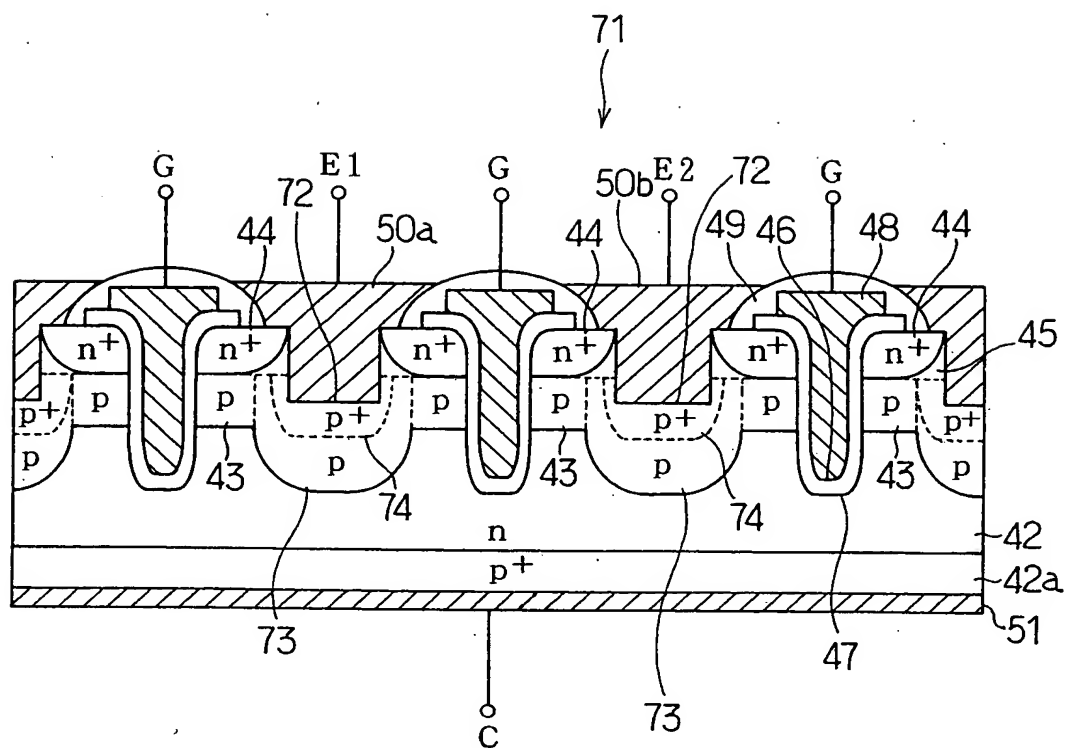


FIG. 8A

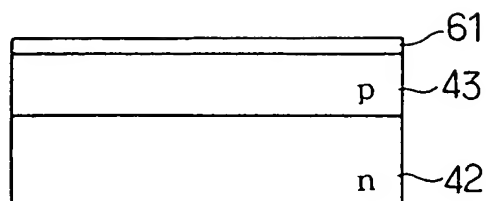


FIG. 8B

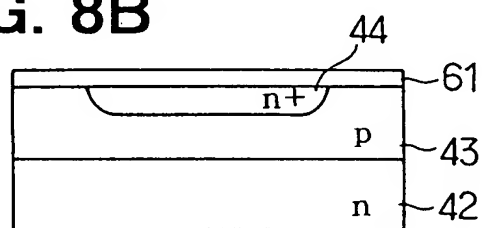


FIG. 8C

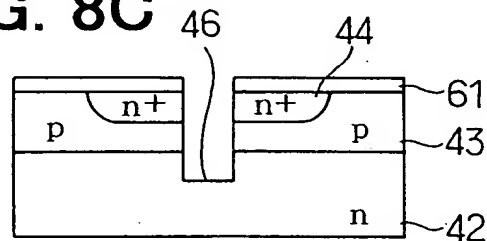


FIG. 8D

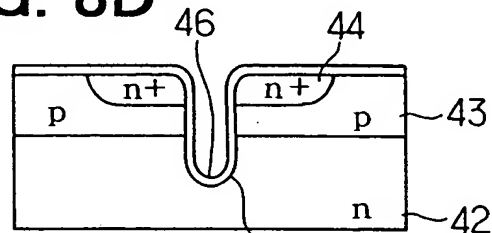


FIG. 8E

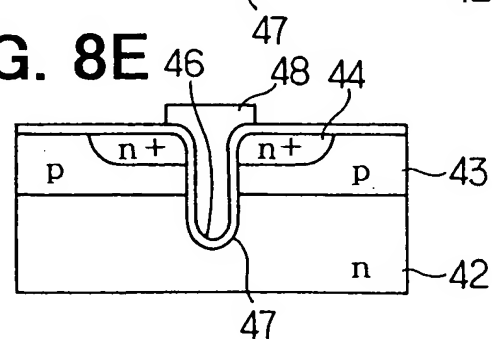


FIG. 8F

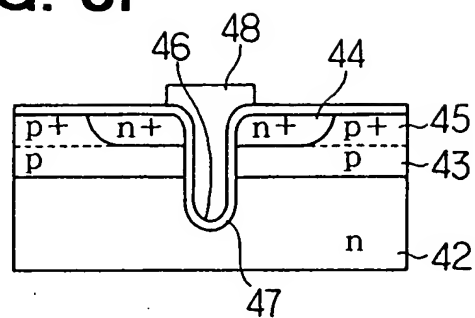


FIG. 8G

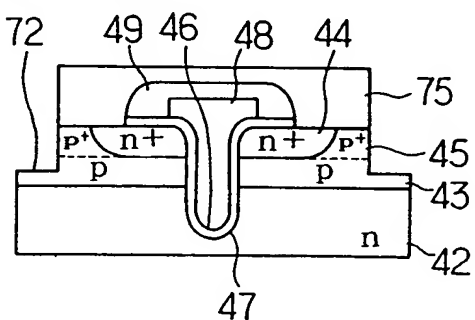


FIG. 9A

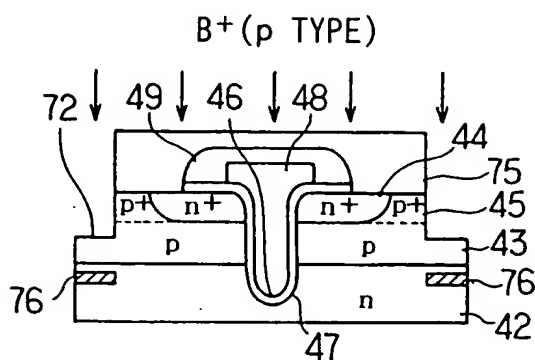


FIG. 9D

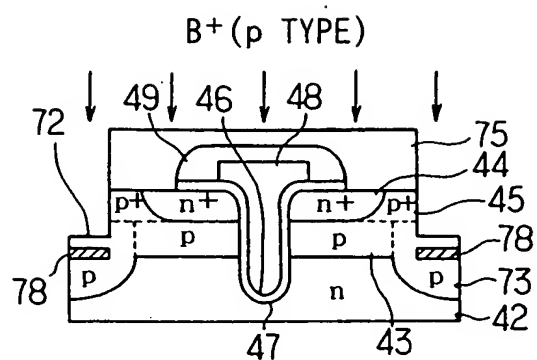


FIG. 9B

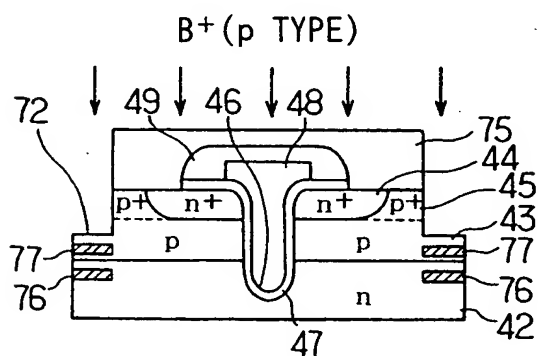


FIG. 9E

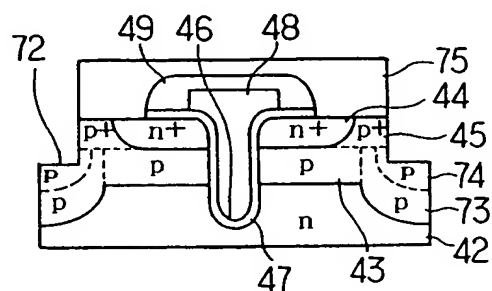


FIG. 9C

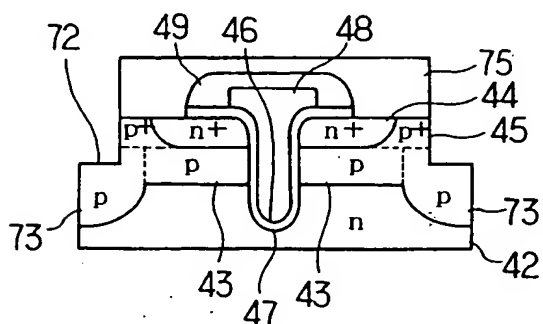


FIG. 9F

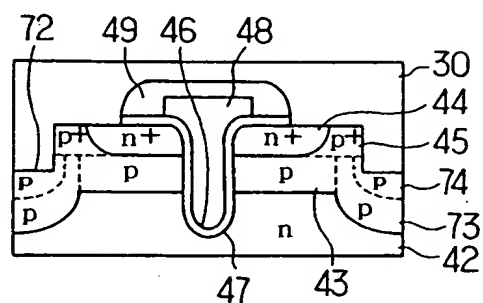


FIG. 10

A cross-sectional view of a semiconductor device, labeled FIG. 10. The device consists of a substrate 30 with a p-type region 43. A gate electrode 81 is positioned on top of the substrate, with a gate oxide layer 44 and a gate stack 46. The gate stack 46 is composed of a p+ region 72, a p region 74, and a p region 73. The gate oxide layer 44 is formed on the p+ region 72, the p region 74, and the p region 73. The p+ region 72 is doped with n+ ions. The p region 74 is doped with p+ ions. The p region 73 is doped with p ions. The p region 43 is doped with p ions. The substrate 30 is doped with p ions. The device is shown with three gate electrodes 81, each with a gate oxide layer 44 and a gate stack 46. The gate stacks 46 are connected to a common gate electrode 81. The gate oxide layer 44 is formed on the p+ region 72, the p region 74, and the p region 73. The p+ region 72 is doped with n+ ions. The p region 74 is doped with p+ ions. The p region 73 is doped with p ions. The p region 43 is doped with p ions. The substrate 30 is doped with p ions. The device is shown with three gate electrodes 81, each with a gate oxide layer 44 and a gate stack 46. The gate stacks 46 are connected to a common gate electrode 81. The gate oxide layer 44 is formed on the p+ region 72, the p region 74, and the p region 73. The p+ region 72 is doped with n+ ions. The p region 74 is doped with p+ ions. The p region 73 is doped with p ions. The p region 43 is doped with p ions. The substrate 30 is doped with p ions.

This diagram shows a cross-sectional view of a semiconductor device. It features a central channel region (72) and two side regions (73, 74). The channel region contains a central p+ layer (43) flanked by n+ layers (79). The side regions contain n+ layers (44) flanked by p+ layers (43). The entire structure is enclosed in a p-type substrate (81). Labels 48 and 49 indicate different layers or regions within the device structure.

FIG. 12A

A cross-sectional view of a semiconductor device. The device consists of a substrate 83 with a p-type region 43. On the surface, there are three vertical structures. The left and right structures are identical and consist of a p-type region 48a, an n⁺ region 44, a p⁺ region 43, and an n⁺ region 44. The middle structure is different, consisting of a p-type region 48a, an n⁺ region 44, a p⁺ region 43, and an n⁺ region 44. The middle structure is labeled with 79, 43, 72, and 73a. The substrate is labeled 83. The p-type region is labeled 43. The n⁺ regions are labeled 44. The p⁺ region is labeled 43. The n⁺ region is labeled 44. The p-type region is labeled 48a. The n⁺ region is labeled 44. The p⁺ region is labeled 43. The n⁺ region is labeled 44. The middle structure is labeled with 79, 43, 72, and 73a. The substrate is labeled 83. The p-type region is labeled 43. The n⁺ regions are labeled 44. The p⁺ region is labeled 43. The n⁺ region is labeled 44.

FIG. 13A

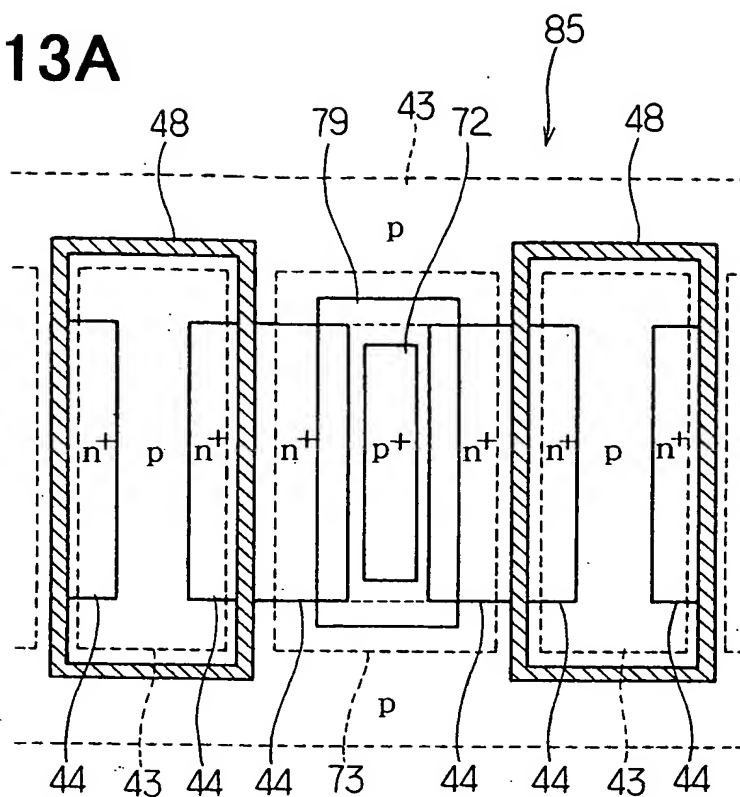


FIG. 13B

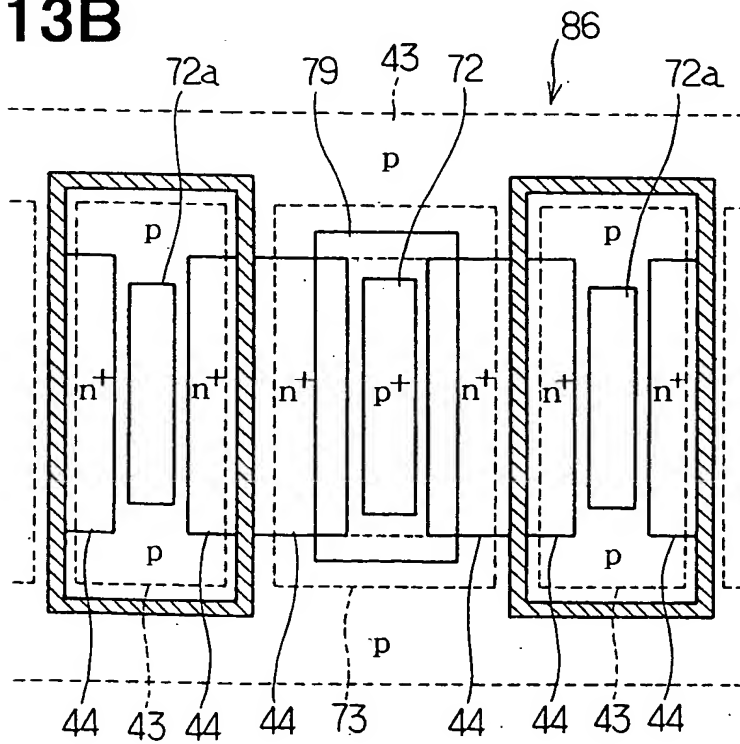


FIG. 14

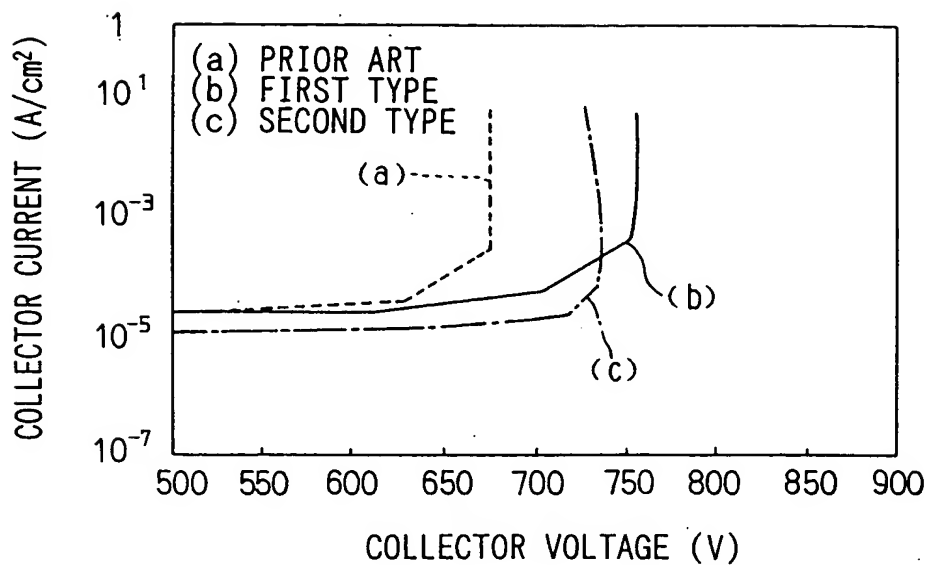


FIG. 16

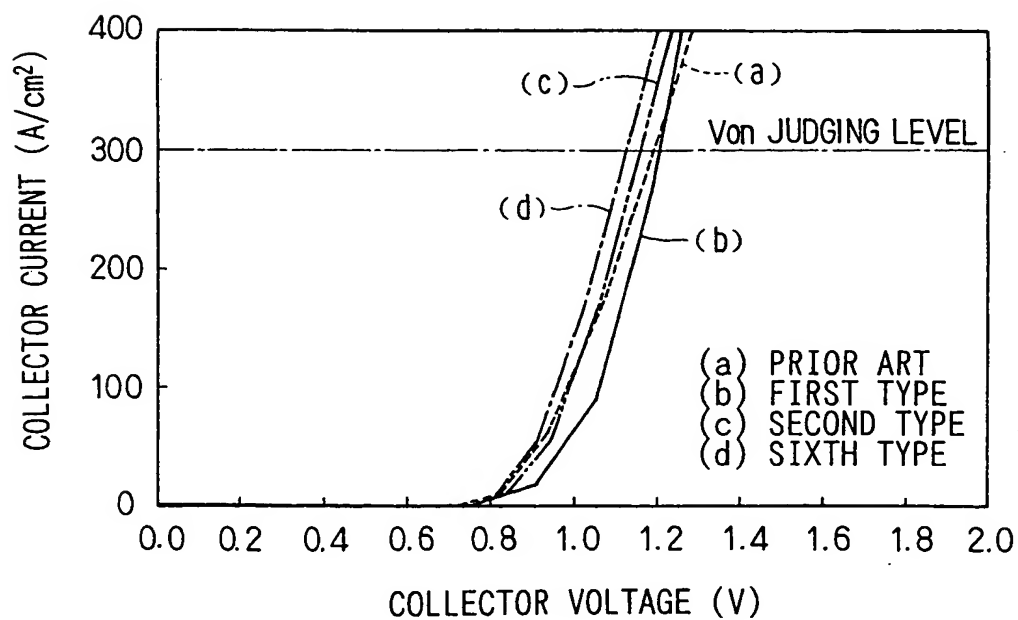


FIG. 15A

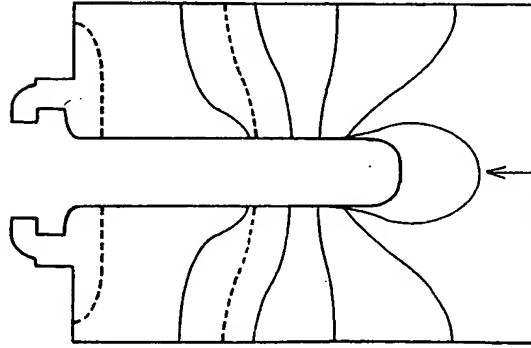


FIG. 15B

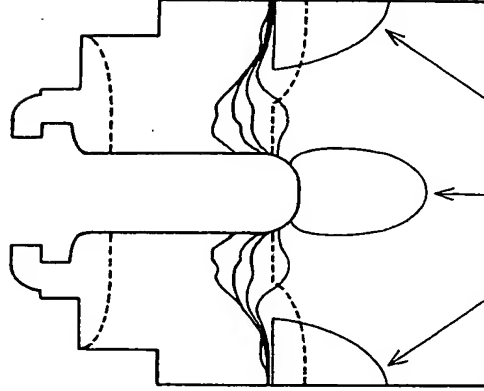
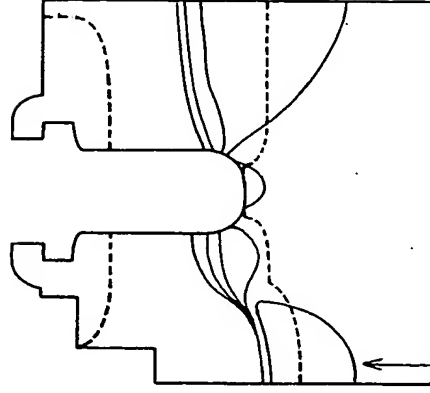


FIG. 15C



ELECTRIC FIELD
CONCENTRATION

ELECTRIC FIELD
CONCENTRATION

ELECTRIC FIELD
CONCENTRATION

FIG. 17

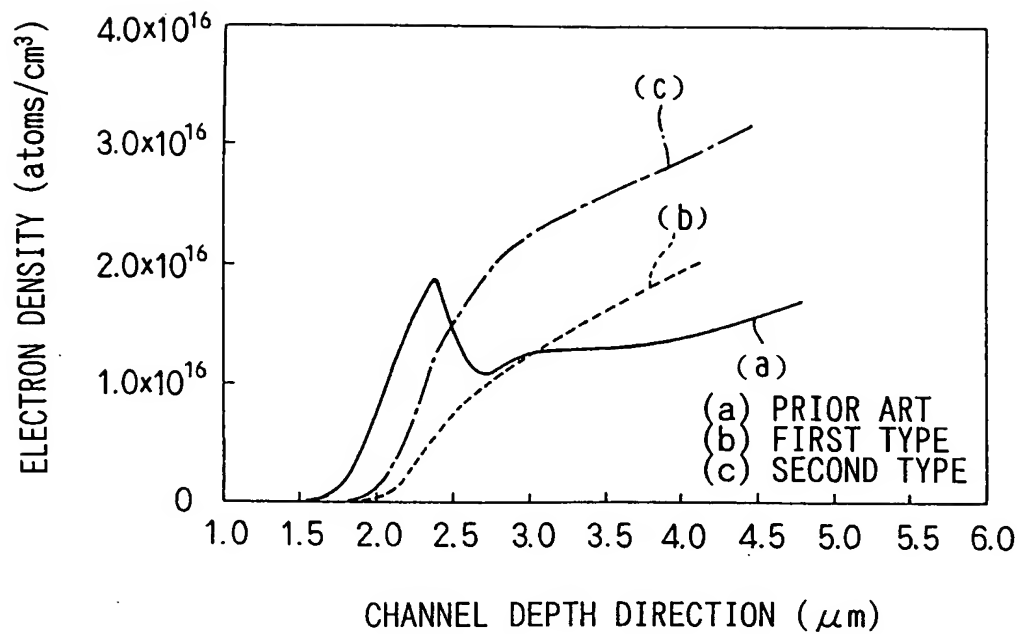


FIG. 19

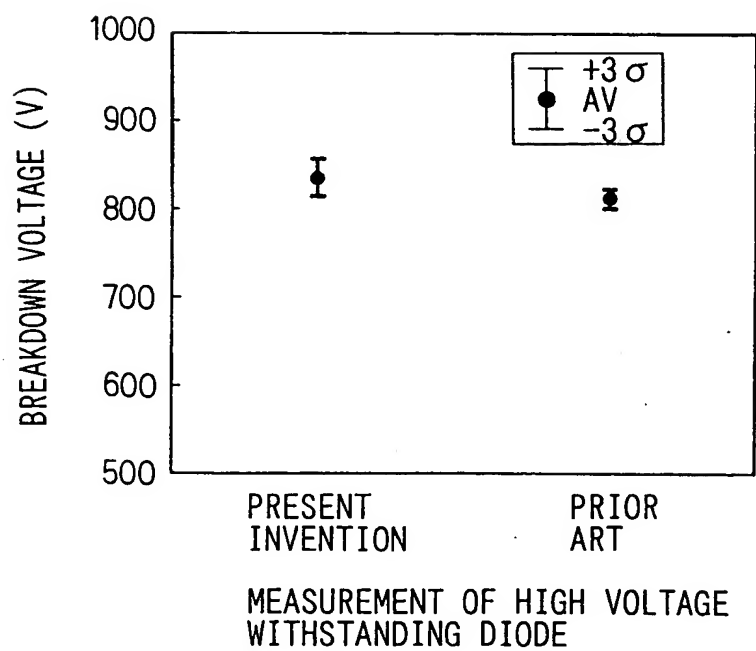


FIG. 18

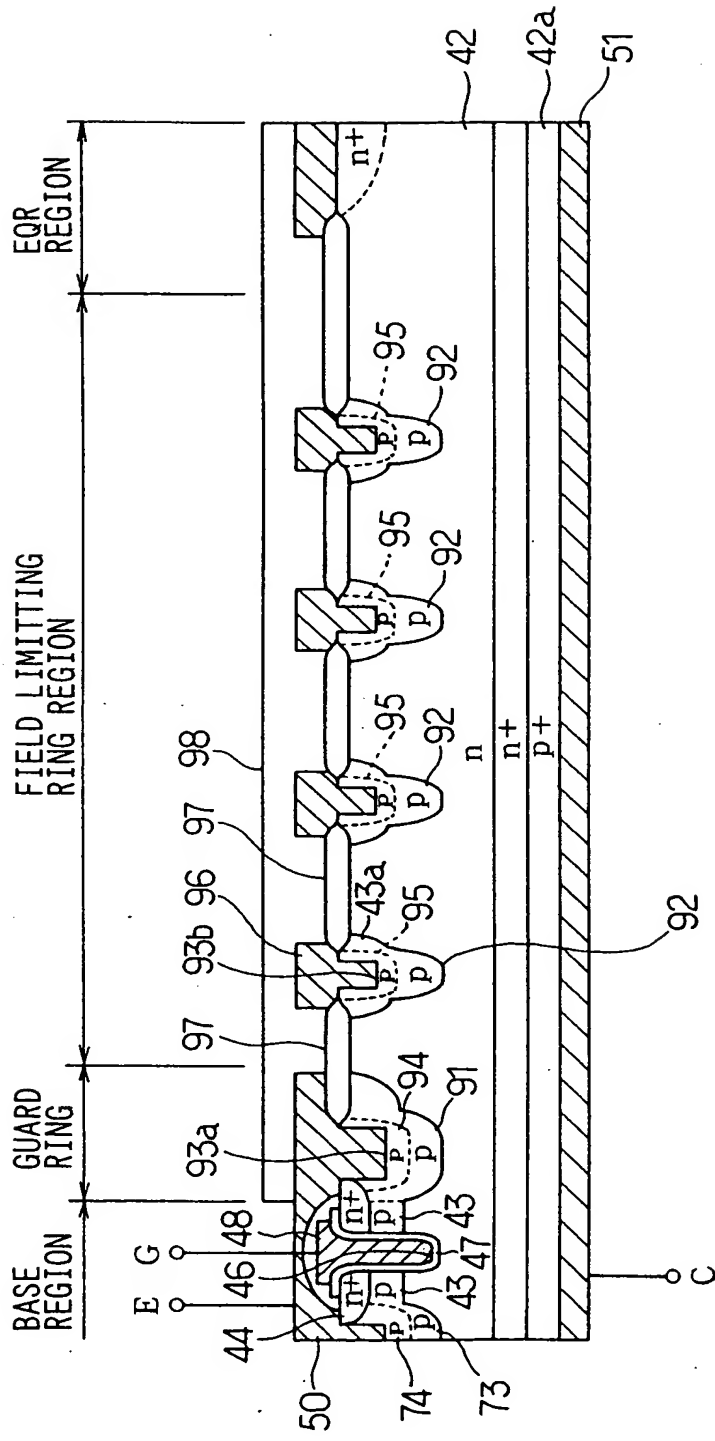


FIG. 20A

PRIOR ART

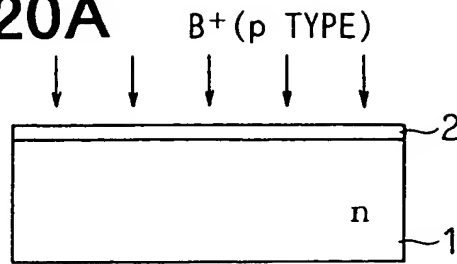


FIG. 20B

PRIOR ART

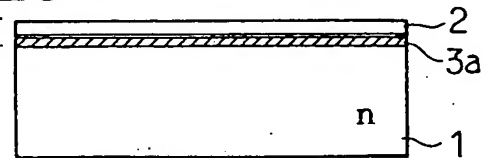


FIG. 20C

PRIOR ART

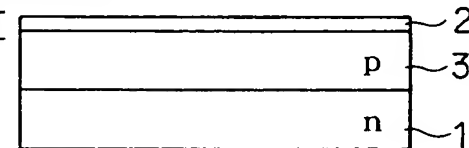


FIG. 20D

PRIOR ART

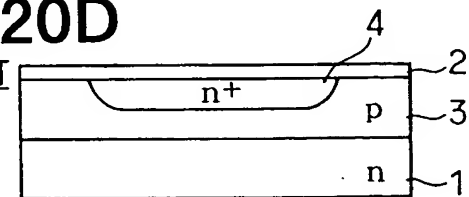


FIG. 20E

PRIOR ART

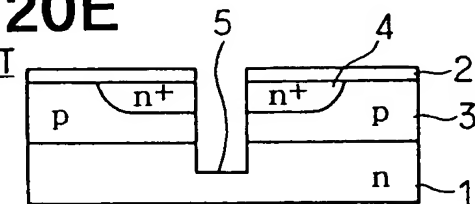


FIG. 20F

PRIOR ART

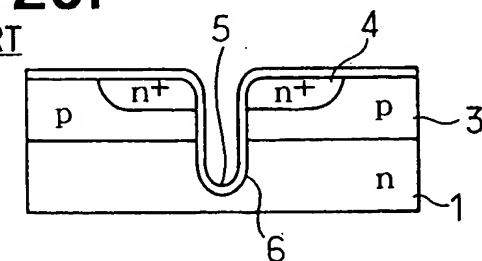


FIG. 20G

PRIOR ART

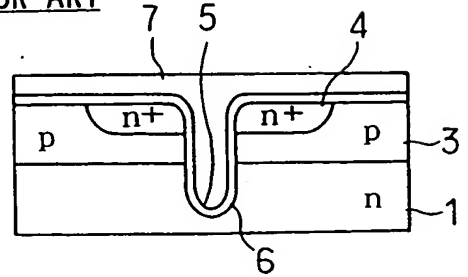


FIG. 20H

PRIOR ART

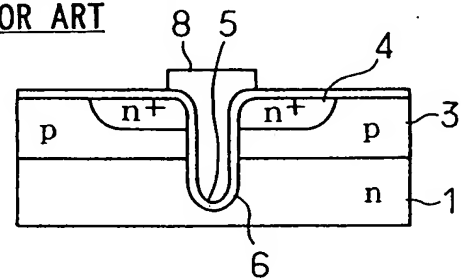


FIG. 20 I

PRIOR ART

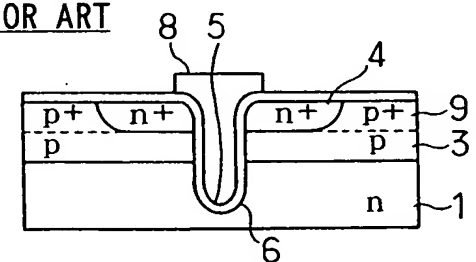


FIG. 20J

PRIOR ART

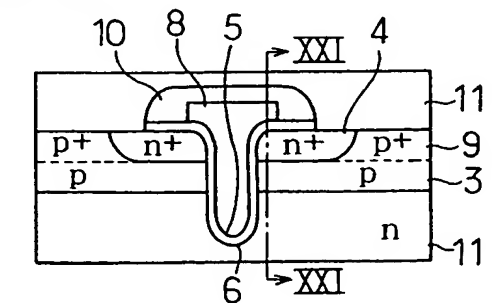


FIG. 21

PRIOR ART

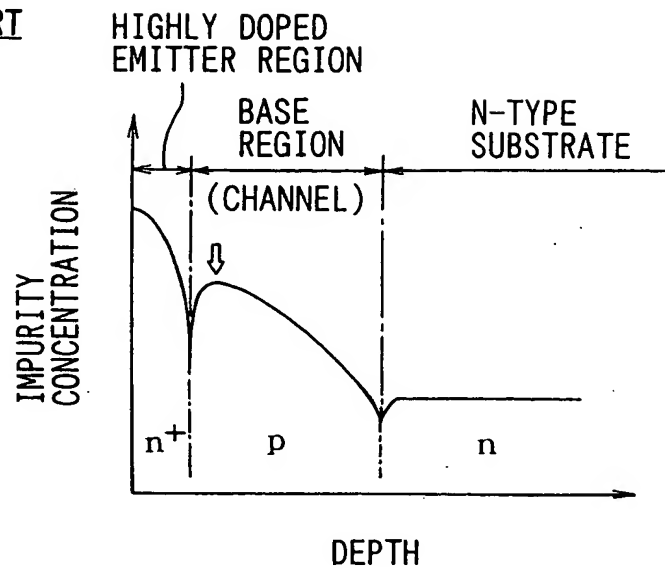


FIG. 22A

PRIOR ART

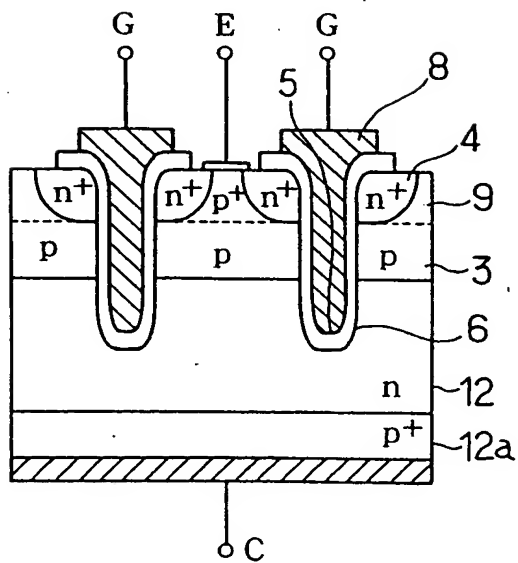


FIG. 22B

PRIOR ART

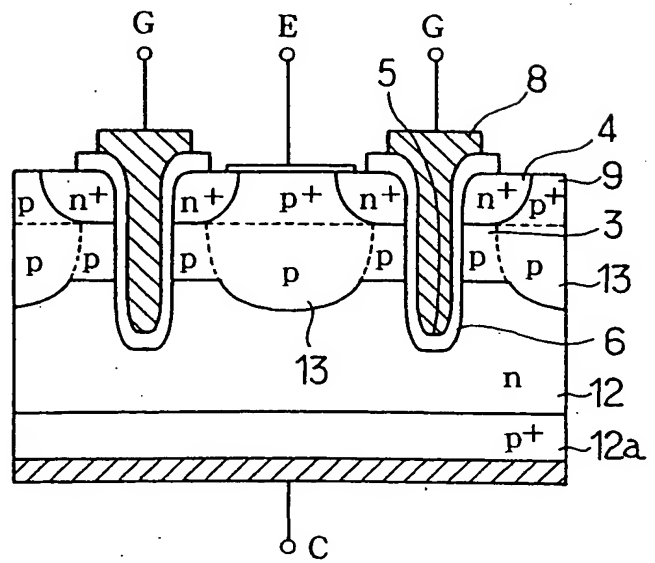


FIG. 23A

PRIOR ART

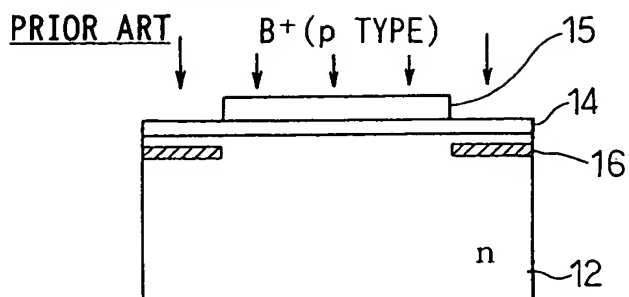


FIG. 23B

PRIOR ART

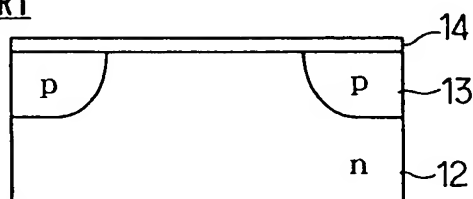


FIG. 23C

PRIOR ART

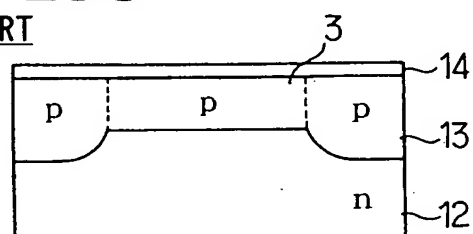


FIG. 23D

PRIOR ART

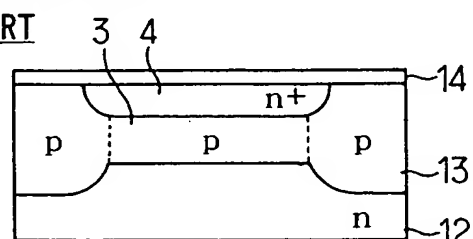


FIG. 23E

PRIOR ART

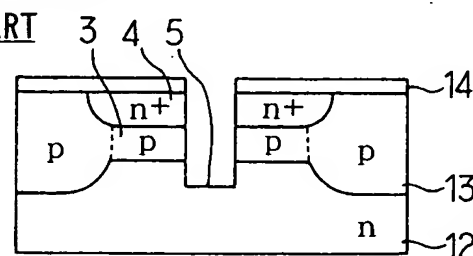


FIG. 23F

PRIOR ART

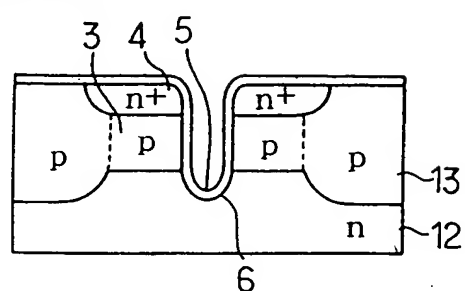


FIG. 23G

PRIOR ART

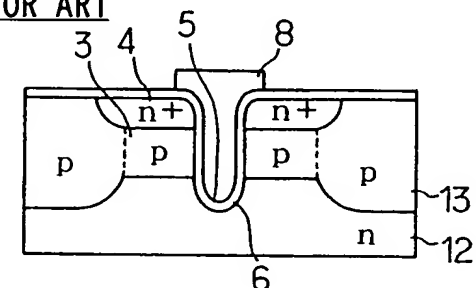


FIG. 23H

PRIOR ART

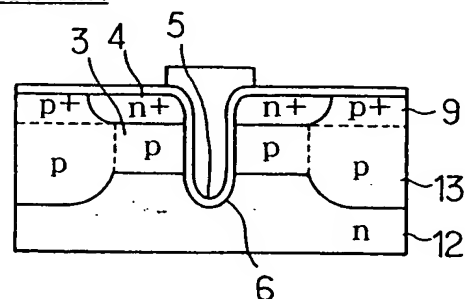


FIG. 23 I

PRIOR ART

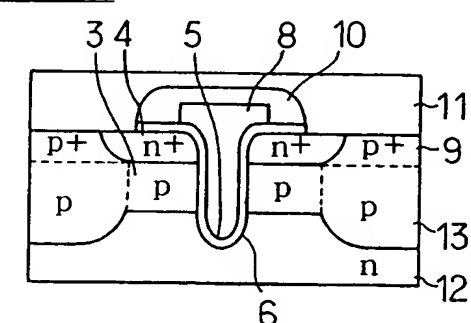


FIG. 24
PRIOR ART

